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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/684,529 | 10/06/2000 | John D. Logue | X-735 US | 1502 |

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XILINX, INC
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| EXAMINER | |
|---|---|
| ZHENG, EVA Y | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2611 | |

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/684,529 | LOGUE ET AL. | |
| | Examiner | Art Unit | |
| | Eva Yi Zheng | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5-7,9-18 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,9,12,13,18 and 23* is/are rejected.

7)☒ Claim(s) *3,10,11 and 14-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/16/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

*Request for Continued Examination*

1. The request filed on February 16, 2006, for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/684,529 is acceptable and a RCE has been established. An action on the RCE follows.

### *Claim Objections*

2. Claims 1 and 23 are objected to because of the following informalities: please add (DFS) abbreviation for digital frequency synthesizer in order to keep consistent with other claims.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 5-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5-7 are depending upon claim 4, which is a cancelled claim.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 5, 9, 12, 13, 18 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (US 6,633,288) in view of Yoon et al. (US 6,445,234), further in view of Ragan et al. (US 6,188,288).

a) Regarding to claim 1, Agarwal et al. disclose an optimum phase and frequency adjustment system, wherein a DLL is coupled to a PLL, which is a frequency synthesizer (406 and 416 in Fig. 4; Col 4, L1-4), wherein the digital frequency synthesizer generates a frequency adjusted clock signal at the frequency adjusted output terminal (HSYNC in Fig. 4). Agarwal et al. disclose all the subject matters above except for the specific teaching of a detailed DLL and frequency synthesizer.

However, Yoon et al. disclose a delay lock loop (DLL) coupled to the reference input terminal (Reference clock in Fig. 1), the skew input terminal (internal clock in Fig. 1), and the output terminal (60 in Fig. 1), wherein the delay lock loop generates an output clock signal at the output terminal (DLL clock in Fig. 1); wherein the delay lock loop comprises a DLL output circuit having a DLL output delay (50 in Fig. 1).

Moreover, Ragan et al. disclose a digital frequency synthesizer (as shown in Fig. 1), and having a variable oscillator (7 in Fig. 1).

Though, Agarwal et al. didn't teach DLL and PLL/frequency synthesizer in details, they are well know technology, and the DLL described by Yoon et al. and the frequency synthesizer described by Ragan et al. have shown specifically. Therefore, it is obvious to one of ordinary skill in art to combine the teaching of Yoon et al. and Ragan et al. with the optimum phase and frequency adjustment system of Agarwal et al. By doing so, synchronize phase and frequency, reduce noise, and produce an optimum communication system.

b) Regarding to claim 2, Yoon et al. disclose wherein the delay lock loop synchronizes a reference clock signal on the reference input terminal with a skewed clock signal on the skew input terminal (as shown in Fig. 1; Col 1, L14-17).

c) Regarding to claim 5, Ragan et al. disclose wherein the digital frequency synthesizer comprise a DFS output circuit having a DFS output delay (as shown in Fig. 1).

d) Regarding to claim 9, Yoon et al. disclose wherein the delay lock loop is configured to generated an output clock signal on the output terminal (DLL clock in Fig. 1), wherein the output clock signal lags the synchronizing clock signal by a DLL output delay (50 in Fig. 1).

e) Regarding to claim 12, Yoon et al. disclose a variable delay circuit coupled between the delay lock loop and the output terminal (50 in Fig. 1).

f) Regarding to claim 13, Ragan et al. disclose a variable delay circuit coupled between the digital frequency synthesizer and the frequency adjusted output terminal (inherent as block 8, 9, 10, 11 shown in Fig. 1).

g) Regarding to claim 18, Ragan et al. disclose wherein the digital frequency synthesizer performs a frequency search (as shown in Fig. 1; abstract), and Yoon et al. disclose the delay lock loop is performing lock acquisition (as shown in Fig.1; abstract).

h) Regarding to claim 23, Agarwal et al. disclose an optimum phase and frequency adjustment system, wherein a DLL is coupled to a PLL, which is a frequency synthesizer (406 and 416 in Fig. 4; Col 4, L1-4), wherein the digital frequency synthesizer generates a frequency adjusted clock signal at the frequency adjusted output terminal (HSYNC in Fig. 4). Agarwal et al. disclose all the subject matters above except for the specific teaching of a detailed DLL and frequency synthesizer.

However, Yoon et al. disclose a delay lock loop (DLL) coupled to the reference input terminal (Reference clock in Fig. 1), the skew input terminal (internal clock in Fig. 1), and the output terminal (60 in Fig. 1), wherein the delay lock loop generates an output clock signal at the output terminal (DLL clock in Fig. 1); wherein the delay lock loop drives a synchronizing clock signal to the frequency synthesizer (inherent a DLL clock in Fig. 1).

Moreover, Ragan et al. disclose a digital frequency synthesizer (as shown in Fig. 1), and having a variable oscillator (7 in Fig. 1).

Though, Agarwal et al. didn't teach DLL and PLL/frequency synthesizer in details, they are well know technology, and the DLL described by Yoon et al. and the frequency synthesizer described by Ragan et al. have shown specifically. Therefore, it is obvious to one of ordinary skill in art to combine the teaching of Yoon et al. and Ragan et al. with the optimum phase and frequency adjustment system of Agarwal et al.

By doing so, synchronize phase and frequency, reduce noise, and produce an optimum communication system.

***Allowable Subject Matter***

7. Claims 3, 10, 11 and 14-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Zheng whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Zheng
Examiner
Art Unit 2611

June 15, 2006

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER